10. (Thrice Amended) An active matrix type display comprising:

a plurality of gate wirings formed on a substrate;

a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a plurality of pixel electrodes formed in a plurality of pixel areas decided by the gate wirings and the data wirings and arranged in a matrix shape;

a thin film transistor formed in each of the pixel areas and structured planar type having an operating semiconductor layer formed on the substrate, a gate insulating film formed on the operating semiconductor layer, a gate electrode formed on the gate insulating film and connected to one of the gate wirings, first and second semiconductor layers having impurity formed on both sides of the operating semiconductor layer, a source electrode including the first semiconductor layer electrically connected to the pixel electrode via a contact window opened to first and second insulating layers laminated on the first semiconductor layer and the gate electrode; and

a plurality of storage capacitor electrodes using the first semiconductor layer as a first storage capacitor electrode, having a second storage capacitor electrode being formed between the first insulating film and the second insulating film and connected to a storage capacitor wiring maintained at a predetermined potential, wherein at least a first storage capacitor is structured by the first storage capacitor electrode, the first insulating film and the

second storage capacitor electrode, and a second storage capacitor is structured by the second storage capacitor electrode, the second insulating film and the pixel electrode.

11. (Amended) An active matrix type display comprising:

a plurality of gate wirings formed on a substrate;

a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a plurality of pixel electrodes formed in a plurality of pixel areas decided by the gate wirings and the data wirings and arranged in a matrix shape;

a thin film transistor formed in each of the pixel areas and structured planar type having an operating semiconductor layer formed on the substrate, a gate insulating film formed on the operating semiconductor layer, a gate electrode formed on the gate insulating film and connected to one of the gate wirings, first and second semiconductor layers formed on both sides of the operating semiconductor layer, a source electrode including the first semiconductor layer electrically connected to the pixel electrode via a contact window opened to first and second insulating layers laminated on the first semiconductor and the gate electrode;

an impurity semiconductor layer formed isolated from the first semiconductor layer on the substrate and made of the same material as the first semiconductor layer; and

a plurality of storage capacitor electrodes using the first semiconductor layer as a first storage capacitor electrode, having a second storage capacitor electrode being formed between the first insulating film and the second insulating film and connected to a storage capacitor wiring maintained at a predetermined potential, wherein at least a first storage capacitor is structured by the first storage capacitor electrode, the first insulating film and the second storage capacitor electrode, and a second storage capacitor is structured by the second storage capacitor electrode, the second insulating film and the pixel electrode.

12. (Amended) An active matrix type display comprising:

a plurality of gate wirings formed on a substrate;

a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a first, a second and a third insulating film formed on the gate wirings;

a pixel electrode formed in a pixel decided by the gate wirings and the data wirings:

a thin film transistor formed in the pixel and having a gate electrode connected to one of the gat wirings, a source electrode connected to the pixel electrode, and a drain electrode connected to the data wirings;

a first storage capacitor electrode formed between the first insulating film and the second insulating film in an area of the gate wiring for previous pixel to the pixel and connected to the pixel electrode; and

second storage capacitor electrode also serving as a storage capacitor wiring formed between the second insulating film and the third insulating film in the area of the gate wiring;

wherein a first storage capacitor is structured by the first storage capacitor electrode, the second insulating film and the second storage capacitor electrode, and a second storage capacitor is structured by the second storage capacitor electrode, the third insulating film and the pixel electrode.

13. (Amended) An active matrix type display as set forth in claim 12, wherein a third storage capacitor is structured by the first storage capacitor electrode, the first insulating film and the gate wiring.

15. (Amended) An active matrix type display as set forth in claim 12, wherein the second storage capacitor electrode also serves as a shading film.

REMARKS

Claim 10 stands rejected under 35 U.S.C. 102(e) as being anticipated by Jung et al. (U.S. 6,317,173). Applicants respectfully traverse this rejection because the cited reference does not disclose (or suggest) a semiconductor layer having impurity being used as a storage capacitor electrode, as in claim 10 of the present invention, as amended.